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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new non-provisional applications under 37 CFR 1 53(b))	Attorney Docket No. 98-0616.01		Total Pages
	First Named Inventor or Application Identifier		
	Vishnu K Agarwal		
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APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.	ADDRESS TO: **Assistant Commissioner for Patents Box Patent Application Washington, DC 20231**

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. ☒ Specification Total Pages 26
(preferred arrangement set forth below)
-Descriptive
-Cross References to Related Application
-Statement Regarding Fed sponsored R & D
-Reference to Microfiche Appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings (if filed)
-Detailed Description
-Claim(s)
-Abstract of the Disclosure
3. ☒ Drawing(s) (35 USC 113) Total Sheets 12 Total Pages 4
4. Oath or Declaration
a. ☐ Newly executed (original or copy)
b. ☒ Copy from a prior application (37CFR 1 63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein

6. ☐ Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☒ 37 CFR 3.73(b) Statement (where there is an assignee) ☒ Power of Attorney
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
12. ☒ Preliminary Amendment
13 ☒ Return Receipt Postcard (MPEP 503)
14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application Status still proper and desired
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
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17. ☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No. ____/________

18. CORRESPONDENCE ADDRESS

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Vishnu K. Agarwal	§	
	§	Group Art Unit:
Serial No.:	§	
	§	Examiner:
Filed: August 31, 2000	§	
	§	Atty. Docket: 98-0616.01
For: DEVICE AND METHOD FOR PROTECTING	§	
AGAINST OXIDATION OF A CONDUCTIVE LAYER IN	§	
SAID DEVICE	§	

PRELIMINARY AMENDMENT

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Dear Sir:

After awarding the above-captioned application the benefit of the priority date of its parent -- application #09/200,253, filed November 25, 1998 -- please amend the current application as follows.

IN THE SPECIFICATION:

Immediately after the title, please add the following: --

Related Application

This application is a divisional of U.S. application Ser. No. 09/200,253, filed Nov. 25, 1998. --

IN THE CLAIMS:

Please cancel claims 1-72 without prejudice.

REMARKS

Claims 73-75 are the only claims pending as of this Preliminary Amendment. In a restriction required during prosecution of the parent application (see the Office Action of June 20, 2000), the Examiner identified these claims as "Group II" claims "drawn to an in-process device, classified in class 438, subclass 118/622." If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is requested to contact Applicant's undersigned attorney at the number indicated.

Respectfully submitted,

Date: 8|31|00

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DOCKET NO 98-0616

APPLICATION FOR LETTERS PATENT

FOR

DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE

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DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE

Technical Field

The present invention relates generally to a method of protecting against a conductive layer incorporating oxygen and a device including that layer. More specifically, the present invention relates to an *in situ* treatment of tungsten nitride.

Background of the Invention

There is a constant need in the semiconductor industry to increase the number of dies that can be produced per silicon wafer. This need, in turn, encourages the formation of smaller die. Accordingly, it would be beneficial to be able to form smaller structures and devices on each die without losing performance. For example, as capacitors are designed to take an ever decreasing amount of die space, those skilled in the relevant art have sought new materials with which to maintain or even increase capacitance despite the smaller size.

One such material is tantalum pentoxide (Ta_2O_5), which can be used as the dielectric in the capacitor. Oftentimes, an electrically conductive layer, such as one made of hemispherical silicon grain (HSG), underlies the tantalum pentoxide and serves as the capacitor's bottom conductive plate. With other dielectrics, it is preferable to have a layer of polycrystalline silicon (polysilicon) deposited over the dielectric to serve as the capacitor's top conductive plate. If polysilicon is deposited directly onto tantalum pentoxide, however, several problems will occur. First, silicon may diffuse into the tantalum pentoxide, thus degrading it. Second, oxygen will migrate from the tantalum pentoxide, resulting in a capacitor that leaks charge too easily. Further, the oxygen migrates to the polysilicon, creating a layer of non-conductive oxide, which decreases the capacitance. This can also be a problem when using barium strontium titanate ((Ba, Sr)TiO_3, or BST) as the dielectric.

In order to avoid these problems, it is known to deposit a top plate comprising two conductive layers. Polysilicon serves as the upper layer of the plate, with a non-polysilicon conductive material interfacing between the tantalum pentoxide and polysilicon. One such material often used is tungsten nitride (WN_X, wherein X is a number greater than zero). However, other problems arise with this process. Specifically, by the end of the capacitor formation process, a layer of non-conductive oxide often forms between the two conductive layers of the top plate. For ease of explanation, this non-conductive oxide will be assumed to be silicon dioxide (SiO_2), although other non-conductive oxides, either alone or in combination, may be present.

Without limiting the current invention, it is theorized that the tungsten nitride is exposed to an ambient containing oxygen. The tungsten nitride adsorbs this oxygen due to bonds located on the grain boundaries of the tungsten nitride surface. Once the polysilicon layer is deposited, the device is then exposed to a thermal process. For example, the capacitor may be blanketed with an insulator, such as borophosphosilicate glass (BPSG). The BPSG layer may not be planar, especially if it is used to fill a trench in which the capacitor is constructed. Heat is applied to the die to cause the BPSG to reflow and thereby planarize. The heat can cause the oxygen at the tungsten nitride surface to diffuse into the polysilicon, wherein the oxygen and silicon react to form silicon dioxide.

Regardless of the exact manner in which the silicon dioxide layer is formed, the result is that the HSG/Ta_2O_5/WN_X/SiO_2/polysilicon layers form a pair of capacitors coupled in series, wherein the HSG/Ta_2O_5/WN_X layers serve as one capacitor and the WN_X/SiO_2/polysilicon layers serve as the second capacitor in the series. This pair of capacitors has less capacitance combined than the single HSG/Ta_2O_5/WN_X/polysilicon capacitor that was intended to be formed.

Other problems can occur with the association of WN_X and Ta_2O_5. For example, it is possible for the WN_X to serve as the bottom plate of a capacitor, underlying the Ta_2O_5 dielectric. In that case, the deposition of the Ta_2O_5 or a subsequent reoxidation of that layer may cause the WN_X layer to incorporate oxygen, thereby reducing capacitance.

It should be further noted that capacitor formation is not the only circumstance in which such problems can occur. There are many situations in which an in-process multi-layer conductive structure is exposed to oxygen and is subjected to conditions that encourage oxidation. Another example can be seen in the formation of metal lines. A layer of tungsten nitride, or perhaps tantalum nitride, may serve as an interface between the conductive material of a via and the metal line. If the interface is exposed to an ambient containing oxygen, then a thermal process involving the alloying or flowing of the metal in the metal line could cause a similar problem with oxidation, thereby hindering electrical contact.

As a result, there is a specific need in the art to prevent or at least decrease the degradation of capacitance in capacitors and of electrical communication in metal lines. There is also a more general need to prevent or at least protect against or minimize the migration of oxygen in relation to a conductive layer of a semiconductor device.

Summary of the Invention

Accordingly, the current invention provides a method for protecting a conductive layer from oxygen. At least one exemplary embodiment concerns preventing or at least limiting a first conductive layer from incorporating oxygen beneath the layer's surface. Other exemplary embodiments address methods of limiting the first conductive layer's ability to adsorb oxygen. In doing so, such embodiments can help prevent the diffusion of oxygen into a second conductive layer, thereby protecting against oxidation between conductive layers. One such method serving as an exemplary embodiment involves exposing one of the conductive layers to an N_2/H_2 plasma before another conductive layer is provided thereon. In a preferred embodiment, this step is performed *in situ* relative to the environment or ambient atmosphere in which the one conductive layer was provided.

Other exemplary embodiments include the use of other nitrogen-containing plasmas, as well as the use of nitrogen-containing gases that are not in plasma form. Still other exemplary embodiments use gases that do not contain nitrogen.

Further, alternate embodiments protect against oxidation between conductive layers with a step performed *ex situ* relative to the environment or ambient atmosphere in which the one conductive layer was provided. In one specific exemplary embodiment of this type, silane gas is flowed over the one conductive layer.

In preferred exemplary embodiments, at least one of the processes described above is performed on a conductive material that has the ability to adsorb or otherwise associate with oxygen. In a more specific embodiment, this material is a non-polysilicon material. Still more specific exemplary embodiments perform one of the processes on tungsten nitride or on tantalum nitride. In an even more specific exemplary embodiment, a tungsten nitride layer is treated before providing a polysilicon layer thereover.

In yet another exemplary embodiment, a treatment such as the ones described above occurs in the context of capacitor formation and, more specifically, occurs in between depositing two conductive layers serving as the capacitor's top plate. In another exemplary embodiment, the treatment occurs between depositing the bottom plate and the dielectric of a capacitor. In yet another exemplary embodiment involves treating a conductive layer as part of the formation of a conductive line.

In preferred embodiments, the method completely prevents the formation of the oxidation layer, although other exemplary embodiments allow for the restriction of the oxidation layer. In some embodiments, this oxidation layer is less than 10 angstroms thick. These methods also apply to embodiments concerning limiting a first conductive layer from incorporating oxygen beneath the layer's surface. In addition, the current invention also includes apparatus embodiments exhibiting these characteristics.

Brief Description of the Drawings

Figure 1 depicts an in-process device as known in the prior art.

Figure 2 depicts an in-process device having undergone an additional step known in the prior art.

Figure 3 depicts an in-process device having undergone yet more steps known in the prior art.

Figure 4 depicts one exemplary embodiment of the current invention.

Figure 5 depicts a second exemplary embodiment of the current invention.

Figure 6 depicts an in-process device as known in the prior art.

Figure 7 depicts another in-process device as known in the prior art.

Figure 8 depicts the in-process device in Figure 7 having undergone an additional step known in the prior art.

Figure 9 depicts a third exemplary embodiment of the current invention.

Figure 10 depicts a fourth exemplary embodiment of the current invention.

Detailed Description of the Preferred Embodiment

Figure 1 depicts an "in-process" device 20 – one that is in the process of being constructed – having undergone processes known in the art. First, a substrate 22 has been provided. In the current application, the term "substrate" or "semiconductor substrate" will be understood to mean any construction comprising semiconductor material, including but not limited to bulk semiconductive materials such as a semiconductor wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). Further, the term "substrate" also refers to any supporting structure including, but not limited to, the semiconductive substrates described above. Over the substrate 22, a first conductive layer 24 is provided. It is assumed for purposes of explanation only that the in-process device is a capacitor in the process of being built. Accordingly, the first conductive layer 24 serves as one of the capacitor's conductive plates 25 (see Figure 2) and may be made of HSG. Returning to Figure 1, a dielectric 26 is provided which, in this case, is tantalum pentoxide. Subsequently, a second conductive layer is provided, which is intended to serve as part of the other conductive plate for the capacitor. Because the dielectric 26 is tantalum pentoxide, the second conductive layer should not be polysilicon. Rather, in this case, the second conductive layer is assumed to be a tungsten nitride layer 28. Once the tungsten nitride layer 28 is provided, however, there may be a tendency for oxygen to be adsorbed onto the surface of that layer 28.

Further, this adsorption may occur before a third conductive layer is provided. This layer can be a polysilicon layer 30 illustrated in Figure 2. Ideally, the tungsten nitride layer 28 and the polysilicon layer 30 define the other conductive plate 32.

However, if the third conductive layer is oxidizable, then further process steps may cause other results. For example, as seen in Figure 3, a subsequent thermal process may cause a reaction between the polysilicon layer 30 and the oxygen that had been adsorbed onto the surface of the tungsten nitride layer 28. In building a capacitor, this thermal process can be the reflowing of a BPSG layer 34 that is deposited over the polysilicon layer 30. The heat may cause the formation of a silicon dioxide layer 36 between the tungsten nitride layer 28 and the polysilicon layer 30, essentially creating two capacitors 38 and 40 connected in series and having less combined capacitance than the one capacitor originally intended.

One preferred exemplary embodiment of the current invention is a method for protecting against the formation of the silicon dioxide layer 36 during the formation of the capacitor. Once the prior art steps depicted in Figure 1 are carried out, this exemplary embodiment has the tungsten nitride layer 28 exposed *in situ* to an N_2 and H_2 plasma. The term *in situ* indicates that the plasma process takes place in the same chamber, or at least within the same general atmosphere, as the process used to provide the tungsten nitride layer. At the very least, the term *in situ* indicates that the plasma process takes place before exposing the in-process device 20 to the atmosphere associated with providing the polysilicon layer 30. Exemplary process parameters include a temperature ranging from about 150 to about 600 degrees Celsius; gas flows including H_2 at about 50 to about 2000 sccm, N_2 at about 5 to about 1000 sccm, and Ar at about 200 to about 2000 sccm; a radio frequency (RF) power ranging from about 50 to about 1000W; a pressure ranging from about 1 millitorr to about 10 torr; and a process time ranging from about 10 seconds to about 240 seconds. One of ordinary skill in the art, however, can appreciate that these parameters can be altered to achieve the same or a similar process.

Without limiting the current invention, it is theorized that this treatment stuffs the tungsten nitride grain boundaries with nitrogen or otherwise passivates the layer, thereby making the bonds at the grain boundaries less active. As a result, oxygen will be less

likely to be adsorbed or otherwise become associated with the tungsten nitride layer, if at all. For example, without this treatment, a silicon dioxide layer 36 about 10 to 40 angstroms thick will form between the tungsten nitride layer 28 and the polysilicon layer 30 (see Figure 3). The exemplary process described above can result in a silicon dioxide layer 36 that is less than 10 angstroms thick, as seen in Figure 4, and is preferably non-existent, as illustrated in Figure 5.

Moreover, the current invention is not limited to the process described above. There are other methods of providing nitrogen to the tungsten nitride that are within the scope of this invention. For example, another such plasma treatment involves the use of ammonia (NH_3) in place of the nitrogen and hydrogen. In using ammonia for the plasma, parameters such as the ones previously described can be used, except that it is preferred to have a flow rate of ammonia ranging from about 5 sccm to about 1000 sccm and a process time of up to 500 seconds. Yet another embodiment includes a plasma treatment using N_2 without H_2. In that case, the exemplary process parameters are generally the same as those used with N_2/H_2 plasma except that the flow rate of N_2 is 50-2000 sccm.

Alternatively, ultraviolet light could be provided in place of RF energy. For example, in using N_2 and H_2 or in using NH_3, the process parameters would be similar to the ones described above for those gases, except the RF energy would be replaced with UV light at a power ranging from 50 W to 3 kW.

Further, the current invention also includes within its scope other methods of providing nitrogen without using electromagnetic energy to affect the gas. One such exemplary embodiment still involves introducing ammonia gas into the process chamber at the same flow rate and time as mentioned in the previous ammonia example, but at a pressure ranging from about 50 millitorr to about 1 atmosphere (760 torr).

In addition, the current invention is not limited to providing nitrogen to the tungsten nitride. Other gases may provide a reducer, passivator material, or some non-oxygen stuffing agent to the tungsten nitride surface; or otherwise cause the tungsten nitride to associate with an oxygen-free material. A plasma treatment using H_2 without N_2 serves as one such embodiment. Exemplary parameters include a temperature ranging from about 150 to about 600 degrees Celsius; gas flows including H_2 at about 50 to about

2000 sccm, and Ar at about 200 to about 2000 sccm; an RF power ranging from about 50 to about 1000W; a pressure ranging from about 1 millitorr to about 10 torr; and a process time ranging from about 10 seconds to about 240 seconds.

Still other gases include diborane (B_2H_6); phosphine (PH_3); and carbon-silicon compounds such as methylsilane (CH_3SiH_3) and hexamethyldisilane $(CH_3)_3Si—Si(CH_3)_3$; and hexamethyldisilazane (HMDS). Additional alternate embodiments of the current invention use hydrazine (N_2H_4), monomethylhydrazine, carbon tetrafluoride (CF_4), CHF_3, HCl, and boron trichloride (BCl_3), which are also useful in passivating dielectrics, as addressed in copending application 09/114,847. Also included are mixtures of any of the gases or types of gases described above. Exemplary non-plasma process parameters using these other gases include a flow rate of about 2 sccm to about 400 sccm for these gases; a flow rate of about 50 sccm to about 100 sccm for an inert carrier gas such as He or Ar; a temperature ranging from about 150 to about 600 degrees Celsius, a pressure ranging from about 50 millitorr to about 1 atmosphere (760 torr); and a process time ranging from about 50 to about 500 seconds. Again, one skilled in the art is aware that these parameters can be altered to achieve the same or a similar process.

It is preferred that at least one of the processes described above occur between providing the tungsten nitride layer 28 and providing the polysilicon layer 30. It is more preferable that one of the inventive processes be carried out in a reducing atmosphere or at least before the tungsten nitride layer 28 is exposed to oxygen. Though such exposure is undesirable in many circumstances, it may be unavoidable. For example, the tungsten nitride layer 28 may be exposed to the cleanroom air at some point during processing. Thus, it is even more preferable to treat the tungsten nitride layer 28 *in situ* relative to the environment or ambient atmosphere used to provide the tungsten nitride layer 28. It is still more preferable to cover the treated tungsten nitride layer 28 before the in-process device 20 is exposed, even unintentionally, to oxygen. This is preferable because any exposure may allow at least some oxygen to associate with the tungsten nitride layer 28, even after one of the inventive treatments disclosed herein. Nevertheless, it is not necessary under the current invention to discourage oxygen adsorption before exposing the in-process device to the atmosphere associated with providing the polysilicon layer

30. If the in-process capacitor 20 is removed from the environment used to provide the tungsten nitride layer 28 and one of the inventive processes described has not been performed, then another option within the scope of the current invention is to expose the tungsten nitride layer 28 to a reducing atmosphere before providing the polysilicon layer 30. This can be done by flowing silane gas (SiH_4) into the environment of the in-process device 20. Process parameters include a silane flow ranging from 50 to 1,000 sccm, a pressure of 10 torr to 1 atmosphere, a temperature ranging from 300 to 700 degrees Celsius, and a process time ranging from 10 to 300 seconds. Moreover, this silane treatment, if chosen, is not limited to *ex situ* situations. Silane gas may be used in place of or in combination with the in situ treatments described herein. Accordingly, any combination of the individual processes covered by the current invention are also within its scope.

As mentioned in the background section, oxygen diffusing away from the tungsten nitride is not the only concern when using that layer along with tantalum pentoxide. As seen in Figure 6, a tungsten nitride layer 128 is deposited over the substrate 122. A dielectric layer 126, assumed to be tantalum pentoxide, is deposited over the tungsten nitride layer 128. Assuming the in-process device of Figure 6 represents the early stage of a capacitor, the tungsten nitride layer 128 will serve as the bottom plate rather than part of the top plate as depicted in previous figures. The process of depositing the tantalum pentoxide dielectric layer 126 may cause the tungsten nitride layer 128 to incorporate oxygen. In addition, further processing, such as a reoxidation of the tantalum pentoxide dielectric layer 126 may cause the tungsten nitride layer 128 to incorporate still more oxygen. This incorporation of oxygen will reduce the capacitance of the finished device. Under these circumstances, a preferred embodiment of the current invention calls for exposing the tungsten nitride layer 128 to an N_2/H_2 plasma before depositing tantalum pentoxide dielectric layer 126. This plasma is created under the parameters already disclosed above. Although using an N_2 and H_2 plasma is preferred, the alternatives presented earlier – such as a non-plasma process, the use of another nitrogen-containing gas, or the use of a nitrogen-free gas, may also be used under these circumstances, and such alternatives fall within the scope of the invention. Further, it is

not required to use tungsten nitride and tantalum pentoxide as the two layers, as embodiments of the current invention will work on other conductive layers and dielectric layers as well.

Thus, embodiments of the current invention protect against a conductive layer associating with oxygen in at least two circumstances. First, where a dielectric is deposited over a conductive layer, the disclosed methods help prevent oxygen from being incorporated within the conductive layer. Second, when a second conductive layer is deposited over the initial conductive layer, the disclosed methods inhibit oxygen from being incorporated by the second conductive layer and forming an oxide.

It should be further noted that embodiments of the current invention are not limited to the circumstances related to the formation of capacitors. As further mentioned in the background section, a similar risk of oxidation between two conductive materials can occur during the formation of metal lines in a semiconductor device. As seen in Figure 7, insulation 42 has been deposited over the substrate 22 and subsequently etched to define a via 44. The via is filled with a conductive material, such as polysilicon, tungsten, copper, or aluminum. In this configuration, the conductive material may be referred to as a "plug" 46. The plug 46 will allow electrical communication between the underlying substrate 22, which may be doped to serve as part of a transistor, and the overlying line material 48. The line material 48 may be copper or some other conductive material, including an alloy. The line material 48 is often deposited within a container 50, also defined by etching insulation 42. (One skilled in the art can appreciate that different layers of insulation may define the via 44 and the container 50.)

As a part of this process, it may also be preferred to include an interposing layer 52 between the line material 48 and the plug 46. For purposes of explaining the current invention, it is assumed that the interposing layer 52 comprises tungsten nitride. This interposing layer 52 may enhance electrical contact between the line material 48 and the plug 46, promote adhesion of the line material 48 within the container 50, prevent or slow the diffusion of material across its boundaries, or serve some other purpose.

Regardless of the intended or inherent purpose, this interposing layer may adsorb oxygen after it is formed. Moreover, there may be thermal processes involved with or

occurring subsequent to providing the line material 48. Such a thermal process could be used to deposit, flow, or alloy the line material 48. As a result of this or any other thermal process, it is believed that the oxygen adsorbed by the tungsten nitride interposing layer 52 will react with the line material 48, thereby forming an oxide layer 54 between the interposing layer 52 and the line material 48 (Figure 8). This oxide layer 54, being an insulator, will hinder the ability to allow electrical communication between the line material 48 and the plug 46. Accordingly, the exemplary methods described above may be used to reduce the oxide layer 54 to a thickness of less than 10 angstroms and preferably down to 0 angstroms, as seen respectively in figures 9 and 10.

One skilled in the art can appreciate that, although specific embodiments of this invention have been described for purposes of illustration, various modifications can be made without departing from the spirit and scope of the invention. For example, it is not necessary to use an exemplary treatment of the current invention on a tungsten nitride layer. The invention's embodiments will also be effective on tantalum nitride surfaces, as well as other surfaces that may adsorb or otherwise associate or interact with oxygen.

Further, it should also be noted that the general process described above for providing a metal line could be considered a damascene process, wherein a hole in insulation is filled with metal. This type of process is contrasted to processes wherein a continuous layer of metal is etched to a desired configuration and then surrounded with insulation. More specifically, the metal line process describe above is an example of a dual damascene process. It follows, then, that the current invention may be applied in any type of damascene process. Moreover, one skilled in the art will now be able to appreciate that that exemplary methods embodying the current invention apply to any situation involving the prevention, minimization, or change in a factor affecting the association of oxygen with a conductive layer. As a result, the current invention also includes within its scope devices that comprise two conductive layers and a minimal amount of oxide, if any, therebetween. Accordingly, the invention is not limited except as stated in the claims.

Claims

What is claimed is:

1. A method of treating a semiconductor device, comprising:

providing a capacitor having a first plate, a dielectric over said first plate, and a first conductive layer over said dielectric; and

exposing said first conductive layer to an N_2/H_2 plasma.

2. The method in claim 1, wherein said step of providing a capacitor comprises providing an in-process capacitor; and said method further comprises a step of providing a second conductive layer over said first conductive layer.

3. The method in claim 2, further comprising a step of defining a top plate with said first conductive layer and said second conductive layer.

4. A method of passivating a conductive material, comprising:

providing said conductive material, wherein said conductive material has an ability to associate with oxygen; and

exposing said conductive material to a plasma.

5. The method in claim 4, wherein said step of exposing said conductive material to a plasma causes a reduction in said ability of said conductive material to associate with oxygen.

6. The method in claim 4, wherein said step of exposing said conductive material to a plasma comprises exposing said conductive material to a plasma containing a selection of nitrogen and hydrogen.

7. The method in claim 6, wherein said step of exposing said conductive material to a plasma containing nitrogen comprises exposing said conductive material to a plasma selected from a group consisting of an N_2/H_2 plasma, an N_2 plasma, an H_2 plasma, an NH_3 plasma, and mixtures thereof.

8. The method in claim 7, wherein said step of exposing said conductive material to a plasma containing nitrogen comprises exposing said conductive material to an N_2/H_2 plasma under parameters including:

a temperature ranging from about 150 to about 600 degrees Celsius;
an H_2 gas flow of about 50 to about 2000 sccm;
an N_2 gas flow of about 5 to about 1000 sccm;
an Ar gas flow of about 200 to about 2000 sccm;
an RF power ranging from about 50 to about 1000W;
a pressure ranging from about 1 millitorr to about 10 torr; and
a process time ranging from about 10 seconds to about 240 seconds.

9. The method in claim 7, wherein said step of exposing said conductive material to a plasma containing nitrogen comprises exposing said conductive material to an NH_3 plasma under parameters including:

a temperature ranging from about 150 to about 600 degrees Celsius;
an NH_3 gas flow of about 5 to about 1000 sccm;
an Ar gas flow of about 200 to about 2000 sccm;
an RF power ranging from about 50 to about 1000W;
a pressure ranging from about 1 millitorr to about 10 torr; and
a process time no greater than about 500 seconds.

10. A method of affecting a surface of a conductive layer included as part of a capacitor plate, comprising:

introducing an oxygen-free material to said conductive layer of said capacitor; and
passivating said surface with said oxygen-free material.

11. The method in claim 10, wherein said step of introducing an oxygen-free material comprises introducing a gas containing said oxygen-free material.

12. The method in claim 11, wherein said step of introducing a gas comprises introducing a generally un-ionized gas.

13. The method in claim 12, wherein said step of introducing a generally un-ionized gas comprises providing a nitrogen-free gas.

14. The method in claim 12, wherein said step of introducing a generally un-ionized gas comprises providing a gas selected from a group consisting of ammonia, diborane, phosphine, hydrazine, monomethylhydrazine, carbon tetrafluoride , CHF_3, HCl, boron trichloride, carbon-silicon compounds, and mixtures thereof.

15. The method in claim 14, wherein said step of introducing a generally un-ionized gas comprises providing a gas selected from a group consisting of ammonia, diborane, phosphine, hydrazine, monomethylhydrazine, carbon tetrafluoride , CHF_3, HCl, boron trichloride, methylsilane, hexamethyldisilane, hexamethyldisilazane, and mixtures thereof.

16. The method in claim 15, wherein said step of passivating said surface comprises exposing said surface to an ammonia gas under parameters including:

a temperature ranging from about 150 to about 600 degrees Celsius;
an ammonia gas flow of about 5 to about 1000 sccm;
an Ar gas flow of about 200 to about 2000 sccm;
a pressure ranging from about 50 millitorr to about 1 atmosphere; and
a process time no greater than about 500 seconds.

17. A method of forming a capacitor, comprising:

forming a capacitor plate, comprising:

providing a first conductive layer in a first environment;

exposing said first conductive layer to a passivation gas; and

depositing a second conductive layer over said first conductive layer.

18. The method in claim 17, wherein said step of exposing said first conductive layer to a passivation gas further comprises exposing said first conductive layer to a passivation gas *ex situ*.

19. The method in claim 17, wherein said step of exposing said first conductive layer to a passivation gas further comprises exposing said first conductive layer to silane in a second environment.

20. The method in claim 17, wherein said step of exposing said first conductive layer comprises exposing said first conductive layer to a passivation gas *in situ*.

21. The method in claim 17, wherein said step of exposing said first conductive layer comprises exposing said first conductive layer to a passivation gas while still in said first environment.

22. The method in claim 17, wherein said step of providing a first conductive layer comprises providing a first conductive layer in an oxygen-free environment; and wherein said step of exposing said first conductive layer comprises exposing said first conductive layer to a passivation gas in said oxygen-free environment.

23. The method in claim 22, wherein said step of depositing a second conductive layer comprises depositing said second conductive layer in said oxygen-free environment.

24. The method in claim 22, wherein said step of depositing a second conductive layer comprises depositing said second conductive layer in a second oxygen free-environment.

25. A method of forming a conductive line over a substrate, comprising:

depositing a conductive plug over said substrate;

depositing a nitride over said plug in an ambient atmosphere, wherein said nitride has a surface bond;

treating said surface bond; and

depositing a metal over said nitride.

26. The method in claim 25, wherein said step of treating said surface bond comprises treating said surface bond before said step of depositing a metal.

27. The method in claim 26, wherein said step of treating said surface bond further comprises treating said surface bond in said ambient atmosphere.

28. The method in claim 27, wherein said step of treating said surface bond further comprises treating said surface bond in a reducing atmosphere.

29. The method in claim 28, wherein said step of treating said surface bond further comprises inhibiting an ability of said nitride to adsorb oxygen.

30. A damascene process, comprising:

depositing a first layer of insulation over a substrate;

etching a first hole in said first layer of insulation;

filling said first hole with a metal;

depositing a second layer of insulation over said first layer of insulation;

etching a second hole in said second layer of insulation and over said first hole;

providing an interface layer over said metal and within said second hole; and

exposing said interface layer to a nitrogen/hydrogen plasma.

31. A semiconductor process, comprising:

providing a first conductive layer;

providing a second conductive layer on said first conductive layer; and

inhibiting a formation of oxide between said first conductive layer and said second conductive layer with a passivator material.

32. The process in claim 31, wherein said step of inhibiting a formation of oxide comprises preventing an oxygen molecule from moving from said first conductive layer to said second conductive layer.

33. The process in claim 32, wherein said step of preventing an oxygen molecule from moving from said first conductive layer comprises preventing said oxygen molecule from associating with said first conductive layer.

34. The process in claim 33, wherein said step of providing a first conductive layer further comprises providing a first conductive layer having a bond, wherein said bond has an activity property; and wherein said step of preventing said oxygen molecule from associating with said first conductive layer comprises reducing said activity property.

35. The process in 33, wherein said step of preventing said oxygen molecule from associating with said first conductive layer comprises preventing said oxygen molecule from being adsorbed onto said first conductive layer.

36. A method of forming a semiconductor device, comprising:

depositing a first conductive layer having a surface;

incorporating an oxygen-free material into said surface;

depositing a second conductive layer on said surface; and

exposing said second conductive layer to a thermal process.

37. The method in claim 36, wherein:

said step of depositing a first conductive layer comprises depositing a capacitor plate;

said method further comprises depositing an insulator over said second conductive layer; and

said step of exposing said second conductive layer to a thermal process comprises flowing said insulator.

38. The method in claim 36, wherein:

said step of depositing a first conductive layer comprises depositing a plug; and

said step of exposing said second conductive layer to a thermal process comprises flowing said second conductive layer.

39. The method in claim 36, wherein said step of exposing said second conductive layer to a thermal process comprises exposing said second conductive layer to an alloy process.

40. A method of constructing a multi-layered device, comprising:

providing a first conductive layer in a first environment;

protecting said first conductive layer from oxygen association, wherein said protecting step is accomplished with a second environment formed of a gas selected from a group consisting of:

a plasma,

a non-ionized gas,

a nitrogen-containing gas,

a nitrogen-free gas,

an *in situ* gas,

an *ex situ* gas, and

combinations thereof; and

providing a second conductive layer on said first conductive layer.

41. A method of processing a semiconductor device, comprising:
depositing a first conductive material;
introducing said first conductive material to a nitrogen-containing plasma;
depositing a second conductive material over said first conductive material; and
exposing said first conductive material and said second conductive material to a thermal process.

42. The method in claim 41, wherein said step of exposing said first conductive material and said second conductive material to a thermal process further comprises developing an oxide between said first conductive material and said second conductive material, wherein said oxide is less than 10 angstroms thick.

43. A method of passivating a multilayer conductive structure, comprising:
layering a first conductive material;
introducing a selection of N_2/H_2, N_2, and NH_3 gas to said first conductive material;
releasing nitrogen from said gas with electromagnetic energy; and
layering a second conductive material over said first conductive material.

44. The method in claim 43, wherein said step of releasing nitrogen from said gas with electromagnetic energy comprises directing ultraviolet light toward said gas.

45. A method of treating a wafer, comprising:
depositing a first conductive layer onto said wafer;
exposing said wafer in situ to a reducing environment; and
depositing a second conductive layer.

46. The method in claim 45, wherein said step of exposing said wafer in situ to a reducing environment comprises exposing said wafer to silane gas.

47. The method in claim 46, further comprising a step of exposing said wafer in situ to an N_2/H_2 plasma prior to said step of depositing a second conductive layer.

48. The method in claim 47, wherein said step of exposing said wafer in situ to an N_2/H_2 plasma comprises exposing said wafer in situ to said N_2/H_2 plasma prior to said step of exposing said wafer to silane gas.

49. A method of processing a wafer, comprising:

depositing a first conductive layer having a grain boundary; and

associating a non-oxygen material with said grain boundary by exposing said first conductive layer to a selection consisting of:

an N_2/H_2 plasma,

an N_2 plasma,

an H_2 plasma,

an NH_3 plasma,

an NH_3 non-plasma gas,

a silane gas, and

a combination thereof.

50. The method in claim 49, wherein said step of depositing a first conductive layer further comprises depositing a tungsten nitride layer.

51. The method in claim 50, further comprising a step of depositing a second conductive layer over said first conductive layer.

52. The method in claim 50, further comprising a step of depositing a dielectric over said first conductive layer.

53. The method in claim 52, further comprising:

depositing a second conductive layer over said dielectric; and

exposing said second conductive layer to a selection consisting of:

an N_2/H_2 plasma,

an N_2 plasma,

an H_2 plasma,

an NH_3 plasma,

an NH_3 non-plasma gas,

a silane gas, and

a combination thereof.

54. A method of forming a semiconductor device, comprising:

providing a first conductive layer; and

preventing at least some oxygen from migrating in relation to said first conductive layer.

55. The method in claim 54, wherein said method further comprises providing a dielectric onto said first conductive layer; and wherein said step of preventing at least some oxygen from migrating comprises preventing at least some oxygen from migrating from said dielectric to said first conductive layer.

56. The method in claim 54, wherein said method further comprises providing a second conductive layer onto said first conductive layer; and wherein said step of preventing at least some oxygen from migrating comprises preventing at least some oxygen from migrating from said first conductive layer to said second conductive layer.

57. A semiconductor device, comprising:

a substrate;

a first conductive layer over said substrate;

a dielectric over said substrate;

a second conductive layer over said first conductive layer; and

a non-oxygen material between said first conductive layer and said second

conductive layer.

58. The semiconductor device of claim 57, wherein:

said dielectric is over said first conductive layer;

said second conductive layer is over said dielectric; and

said non-oxygen material is between said first conductive layer and said dielectric.

59. The semiconductor device of claim 57, wherein said first conductive layer is over said dielectric.

60. The semiconductor device of claim 59, further comprising a third conductive layer between said substrate and said dielectric.

61. A capacitor, comprising:

a bottom plate comprising tungsten nitride and having a surface;

nitrogen at said surface;

a dielectric comprising tantalum pentoxide over said surface; and

a top plate over said dielectric.

62. A capacitor, comprising:

a first plate;

a dielectric over said first plate; and

a second plate over said dielectric, comprising:

a first non-polysilicon conductive layer over said dielectric, and

a second conductive layer over said first non-polysilicon conductive layer.

63. The capacitor in claim 62, wherein said dielectric contains oxygen; wherein said first non-polysilicon conductive layer contains nitrogen; and wherein said second conductive layer comprises polysilicon.

64. The capacitor in claim 63, wherein:

said dielectric layer consists of a selection from tantalum pentoxide and barium strontium titanate; and

said first non-polysilicon conductive layer consists of a selection from tungsten nitride and tantalum nitride.

65. The capacitor in claim 64, wherein said second plate comprises an oxygen-free second plate.

66. The capacitor in claim 64, wherein said second plate comprises an oxide layer between said first non-polysilicon conductive layer and said second conductive layer, wherein said oxide layer is less than 10 angstroms thick.

67. The capacitor in claim 64, wherein said first non-polysilicon conductive layer and said second conductive layer are less than 10 angstroms apart and are separated by a silicon dioxide layer.

68. A pair of series-coupled capacitors, comprising:

a first conductive layer;

a dielectric over said first conductive layer;

a second conductive layer over said dielectric;

a third conductive layer less than 10 angstroms over said second conductive layer; and

an oxide of said third conductive layer between said second conductive layer and said third conductive layer.

69. The pair of series-coupled capacitors in claim 68, wherein said first conductive layer, said dielectric, and said second conductive layer define a first capacitor; and wherein said second conductive layer, said oxide, and said third conductive layer define a second capacitor.

70. A semiconductor device, comprising:

a conductive line;

a plug under said conductive line; and

an interposing layer between said conductive line and said plug and comprising a non-oxygen stuffing material.

71. The semiconductor device in claim 70, wherein said interposing layer comprises grain boundaries and nitrogen between said grain boundaries.

72. The semiconductor device in claim 71, further comprising an oxide between said interposing layer and said conductive line.

73. An in-process device, comprising:

a substrate; and

a conductive layer over said substrate and having a surface stuffed with a non-oxygen material.

74. The in-process device of claim 73, wherein said surface is a nitrogen-stuffed surface.

75. The device in claim 74, wherein said surface is contacting an oxygen molecule.

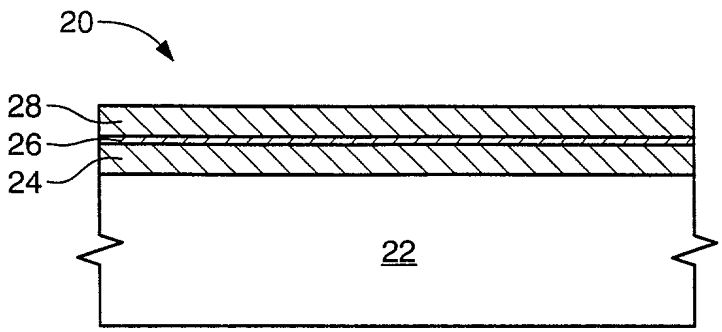

FIG. 1
(PRIOR ART)

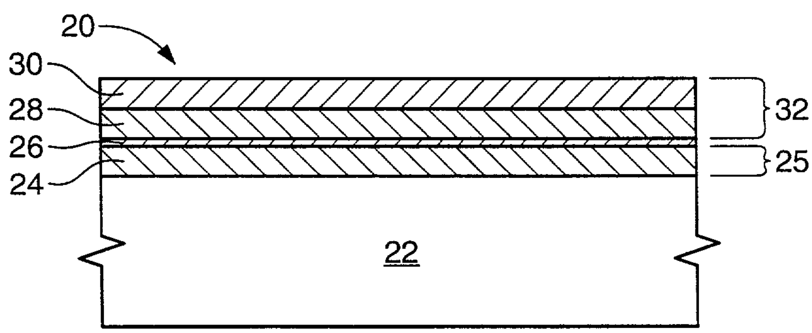

FIG. 2
(PRIOR ART)

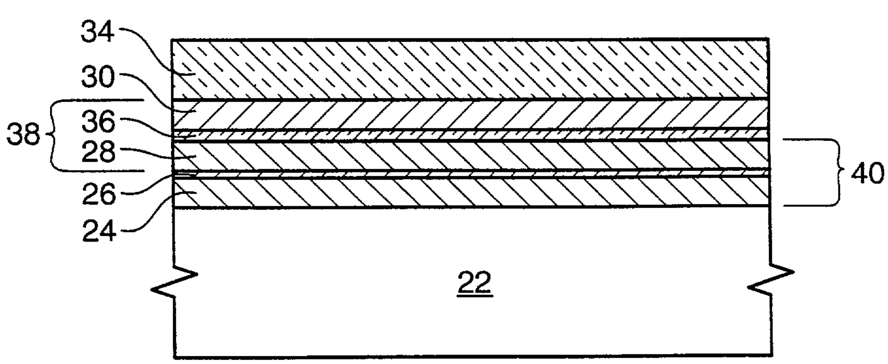

FIG. 3
(PRIOR ART)

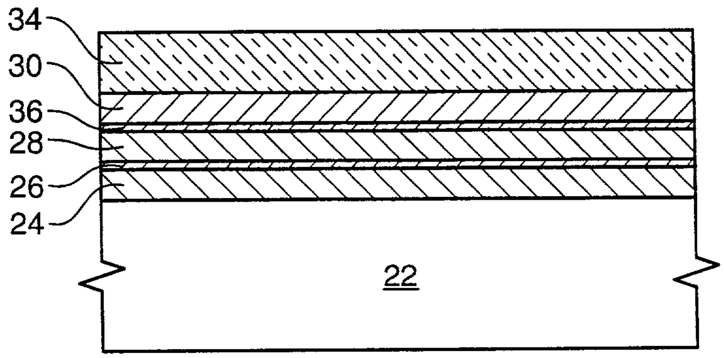

FIG. 4

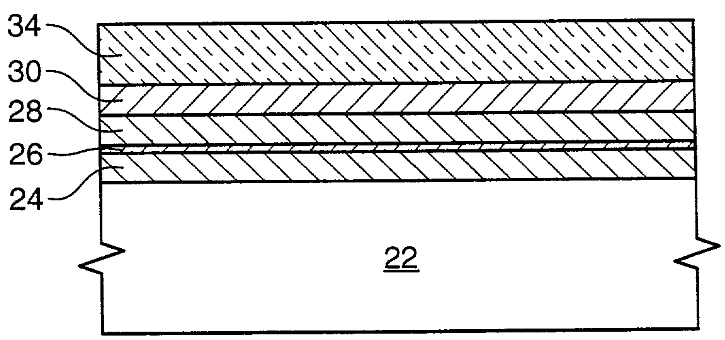

FIG. 5

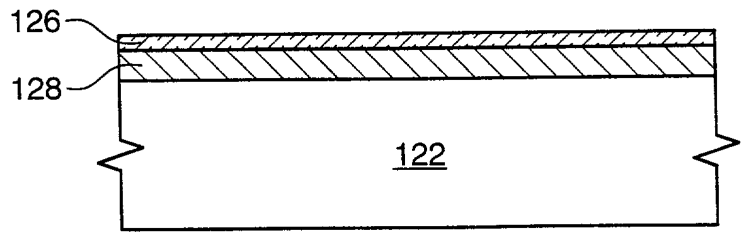

FIG. 6
(PRIOR ART)

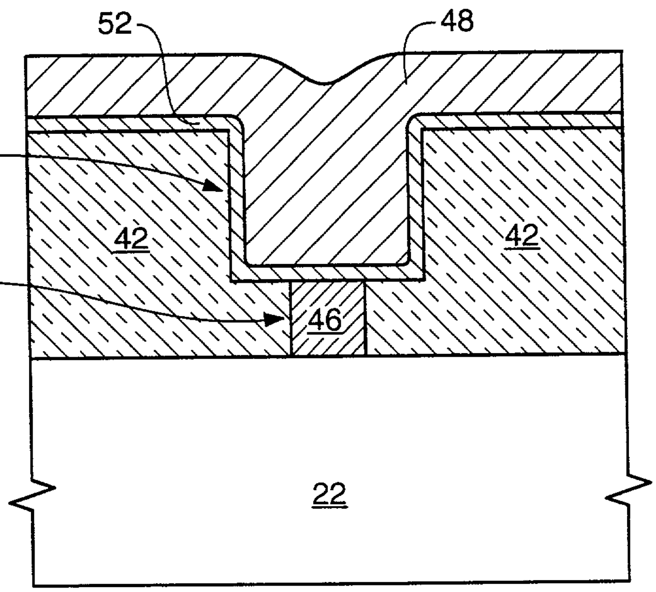

FIG. 7
(PRIOR ART)

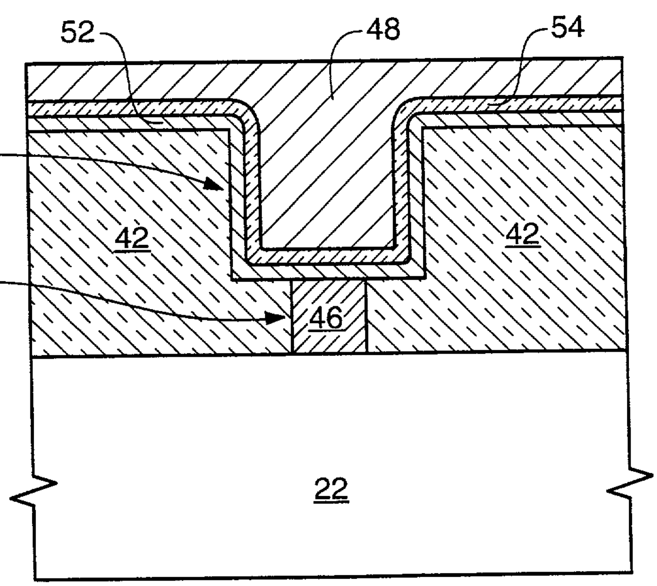

FIG. 8
(PRIOR ART)

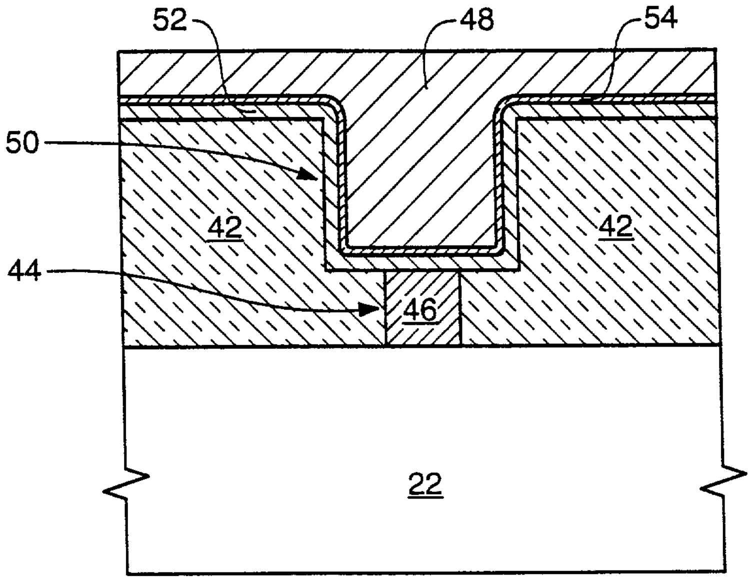

FIG. 9

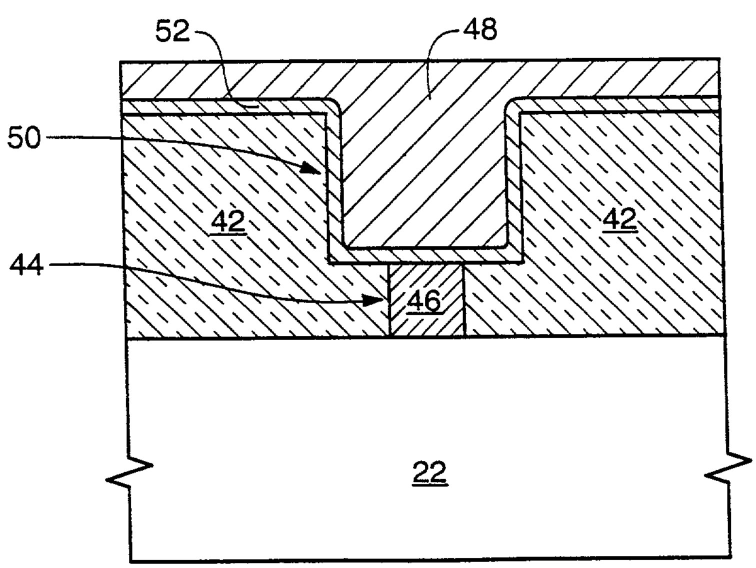

FIG. 10

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE, the specification of which:

_X_ is attached hereto.

___ was filed on __________, as Application Serial No. __________.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability of the subject matter claimed in this application as "materiality" is defined in Title 37 of the Code of Federal Regulations, § 1.56.

I hereby claim the benefit of any earlier filing date in the United States to which I am entitled under Title 35 of the United States Code, § 120 and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 of the United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 of the Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.)	(Filing Date)	(Status)

Send correspondence to:

Charles B. Brantley, II, Mail Stop 525
Micron Technology, Inc.
8000 S. Federal Way
Boise, Idaho 83706
(208) 368-4557

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first or sole inventor: [Vishnu K. Agarwal
]
Inventor's Signature:
(First, ~~Middle Initial~~, Last)
Date: 11|24|98
Residence Address: A303, 2382 E. Red Cedar Lane]
City, State, Country: Boise, ID 83716 United States of America

Citizenship: India
Post Office Address: Same as residence address

Abstract of the Disclosure

In a semiconductor device including a first conductive layer, the first conductive layer is treated with a nitrogen/hydrogen plasma before an additional layer is deposited thereover. The treatment stuffs the surface with nitrogen, thereby preventing oxygen from being adsorbed onto the surface of the first conductive layer. In one embodiment, a second conductive layer is deposited onto the first conductive layer, and the plasma treatment lessens if not eliminates an oxide formed between the two layers as a result of subsequent thermal treatments. In another embodiment, a dielectric layer is deposited onto the first conductive layer, and the plasma treatment lessens if not eliminates the ability of the first conductive layer to incorporate oxygen from the dielectric.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Vishnu K. Agarwal	§	Atty. Docket: 98-0616.01
Serial No.:	§	"EXPRESS MAIL" MAILING LABEL NUMBER EL679497492US
Filed: August 31, 2000	§	DATE OF DEPOSIT 8-31-00
For: DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	§ § § § §	I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R § 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.
		Signature

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below or filed herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Powers of Attorney and appoints: Charles B. Brantley, II, Reg. No. 38,086; Michael L. Lynch, Reg. No. 30,871; Walter D. Fields, Reg. No. 37,130; Kevin D. Martin, Reg. No. 37,882; and David J. Paul, Reg. No. 34,692 as its attorney or agent, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Assignment:

____ Filed concurrently herewith for recording, a copy of which is attached hereto.

_X_ Previously recorded on: 11/25/98, at Reel: 9611, Frame: 0494.

Please direct all communications as follows:

Charles B. Brantley II
Mail Stop 525
MICRON TECHNOLOGY, INC.
8000 S. Federal Way
Boise, ID 83716-9632
(208) 368-4557

ASSIGNEE: MICRON TECHNOLOGY, INC.

Date: 8-31-00

By: __________________
Michael L. Lynch
Chief Patent Counsel